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ABSTRACT

A process for creating a storage node electrode, for a DRAM cell, exhibiting increased surface area resulting from the formation of an agglomerated metal silicide layer, on the top surface of the storage node electrode, has been developed. The process features creating a polysilicon, storage node electrode shape, followed by the formation of an overlying, agglomerated titanium disilicide layer. The agglomerated titanium disilicide layer is formed from a RTA procedure, applied to a smooth titanium disilicide layer, located on the polysilicon, storage node electrode.